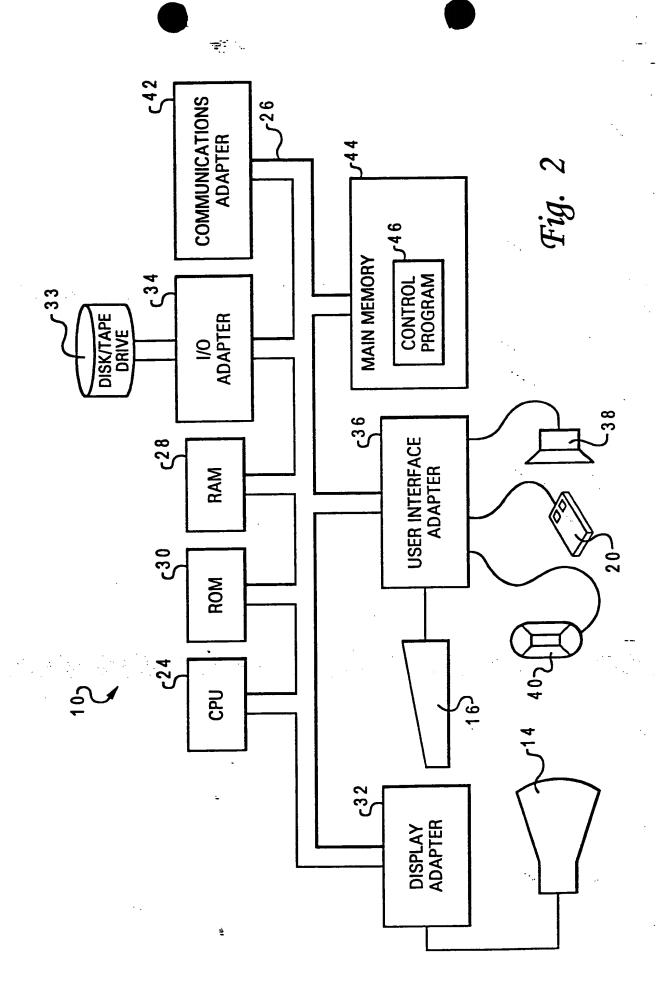


Fig. 1

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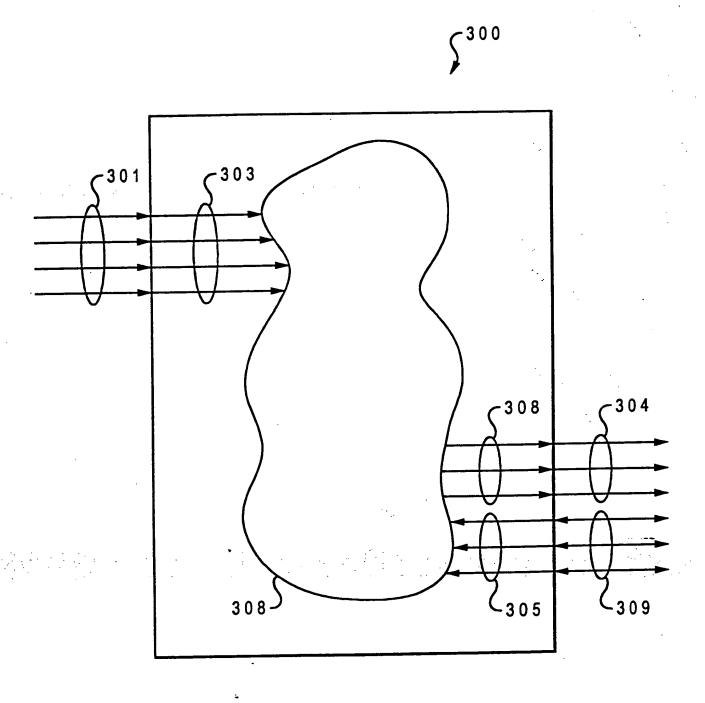
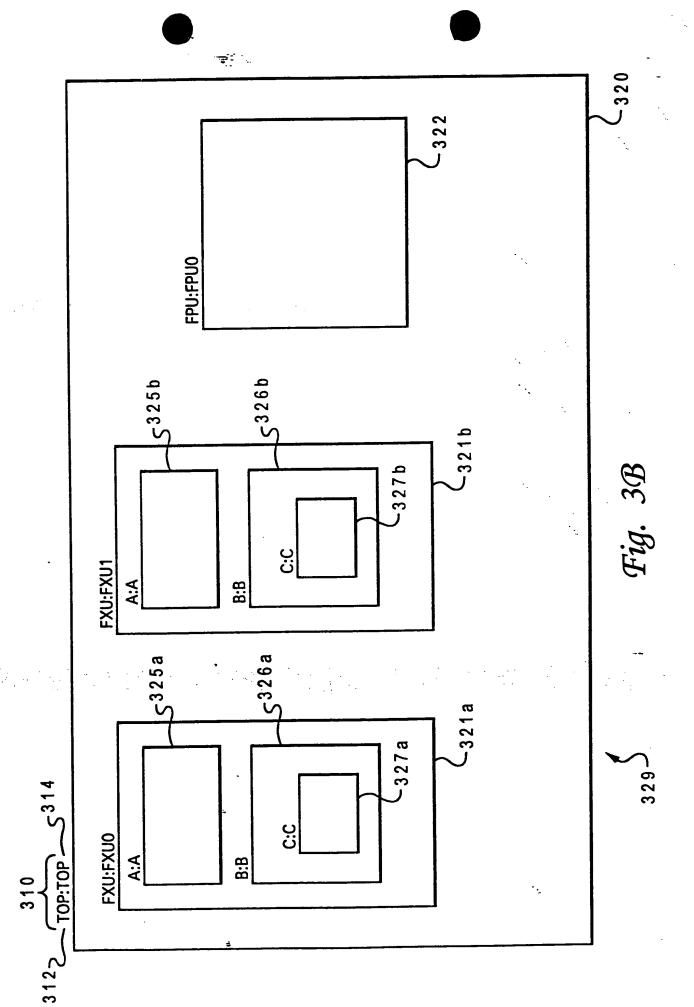
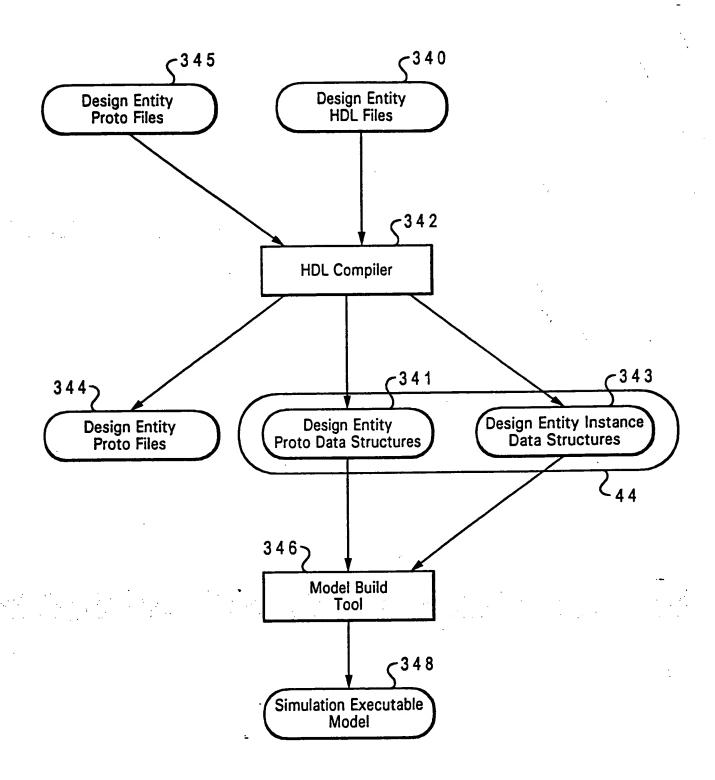


Fig. 3A

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Fig. 3C

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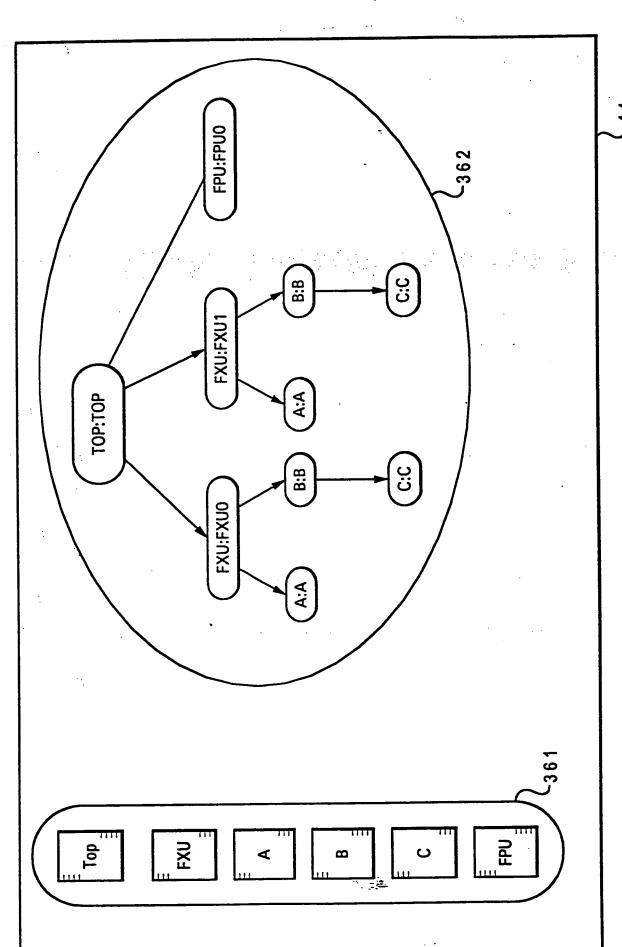


Fig. 3D

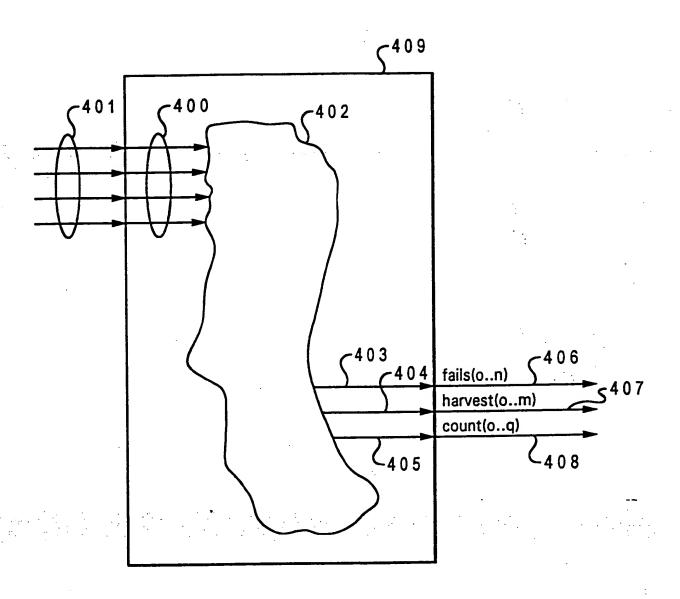
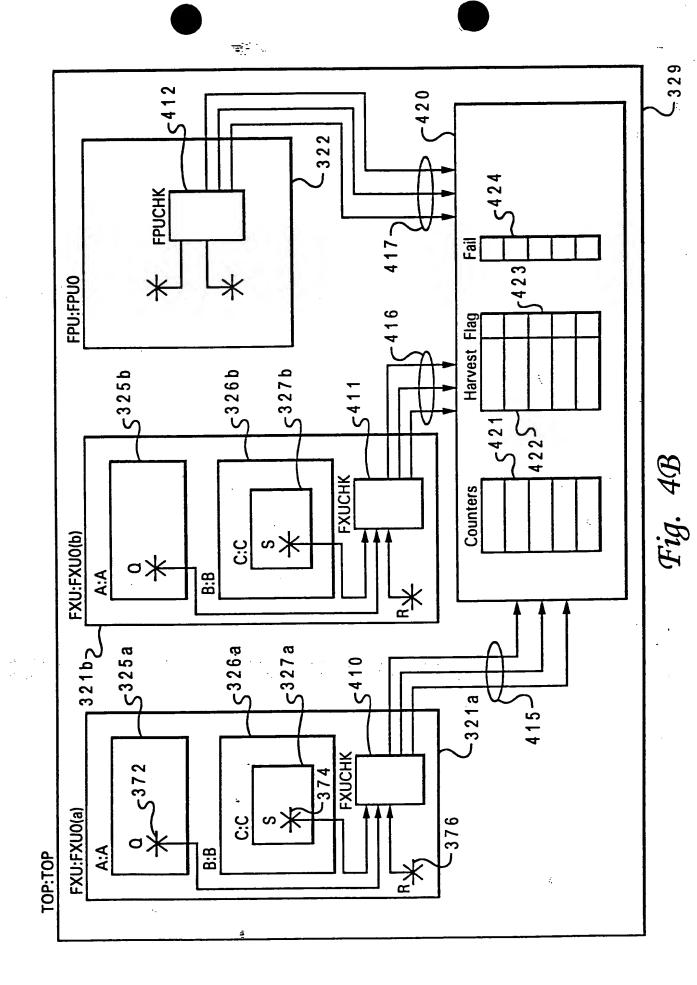


Fig. 4A

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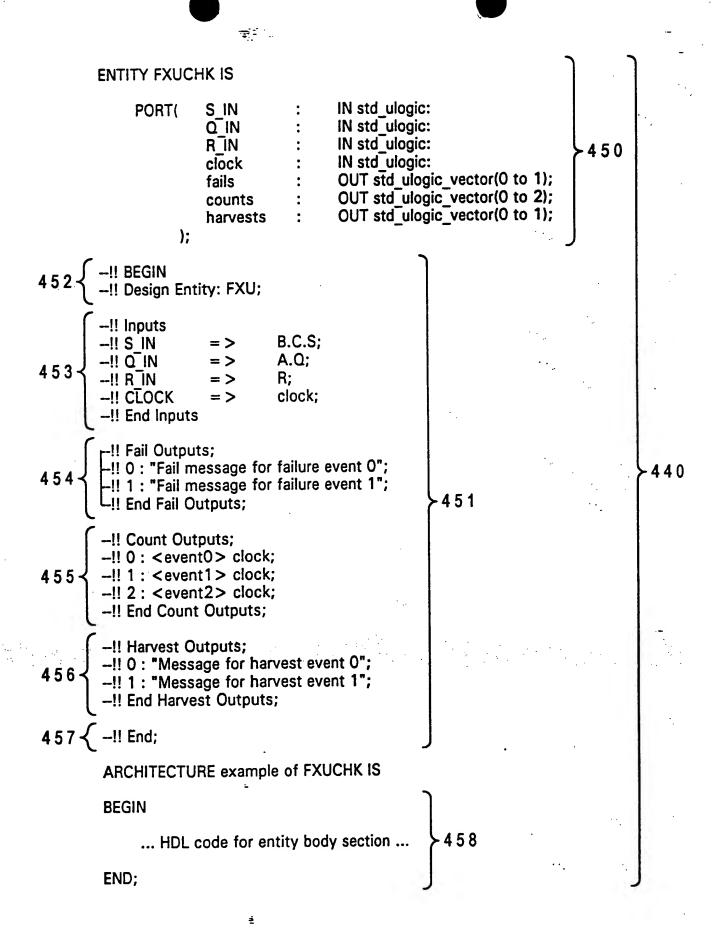
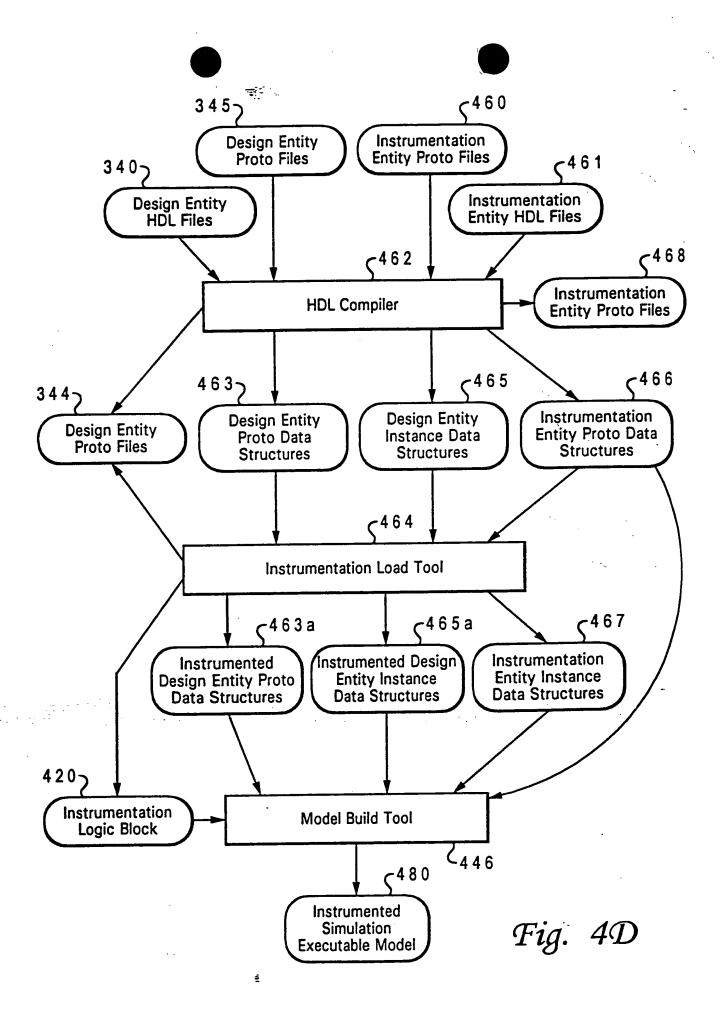


Fig. 4C



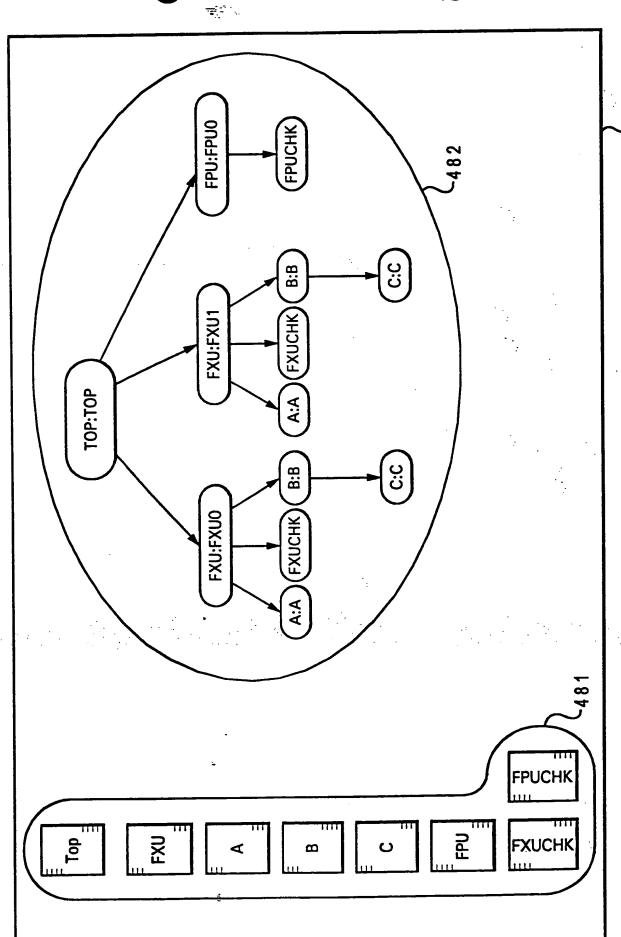
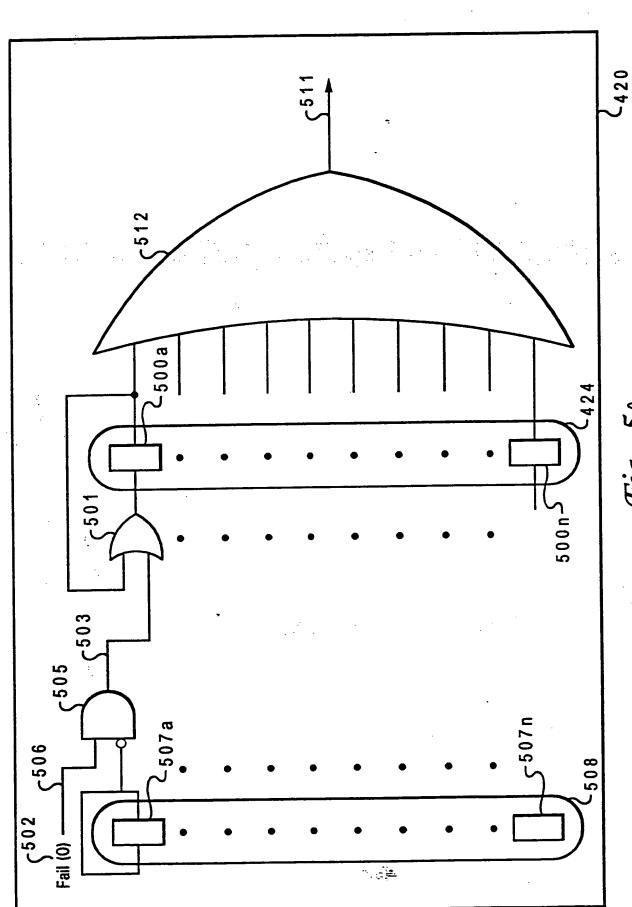


Fig. 49



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Fig. 5A

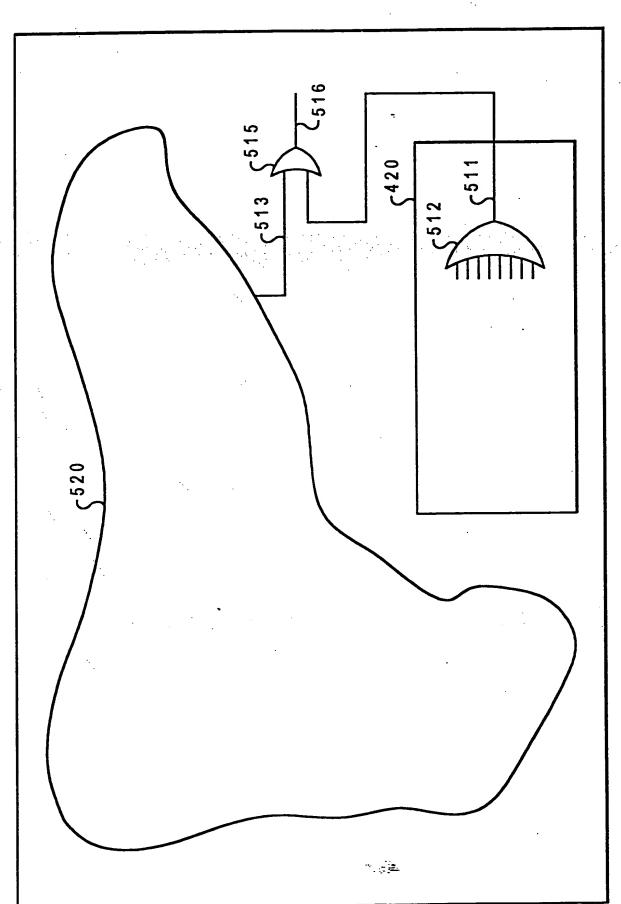
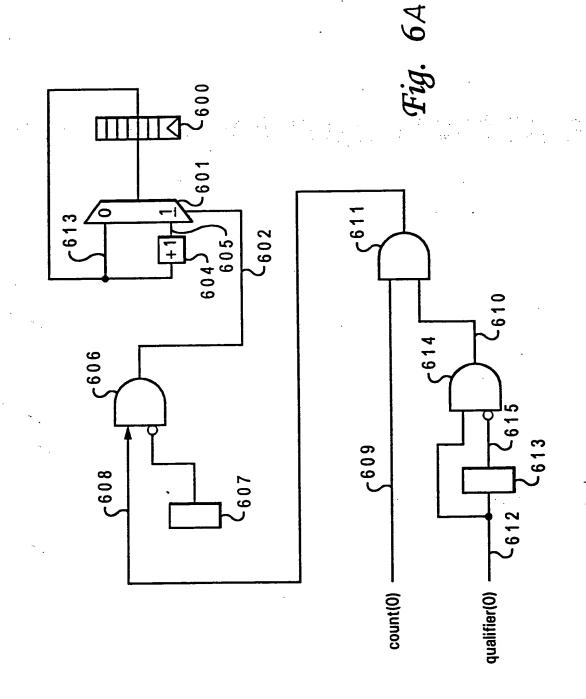
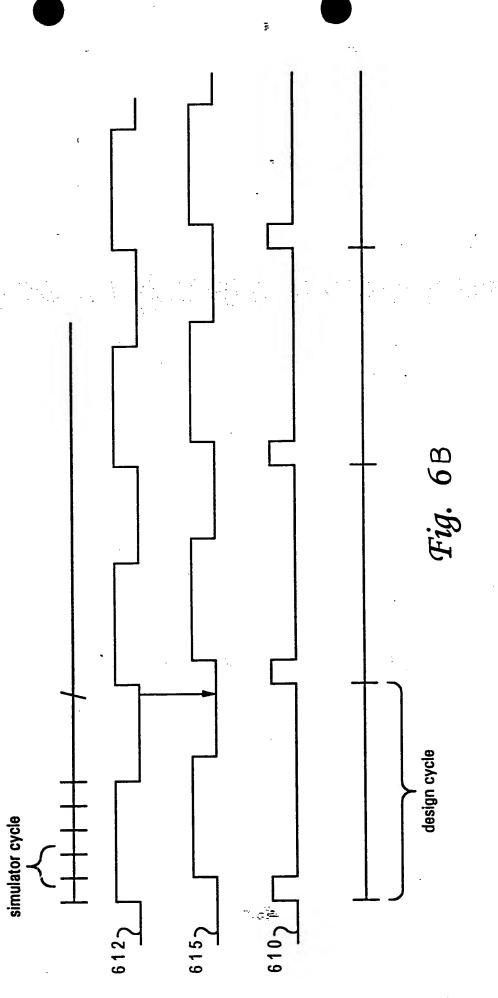


Fig. 5B



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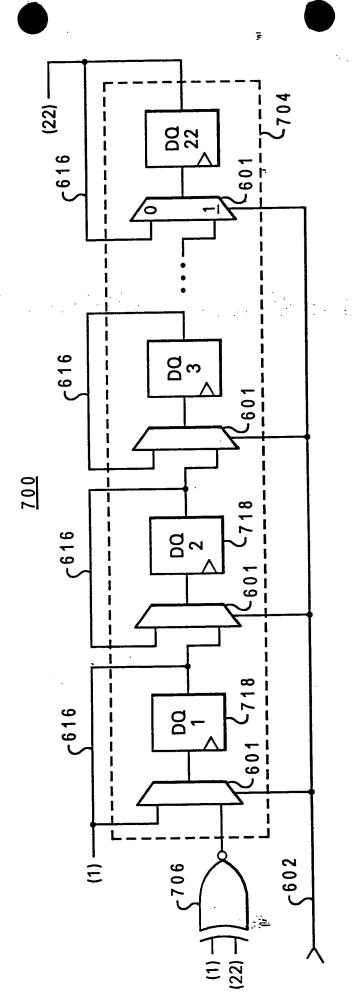


Fig. 7

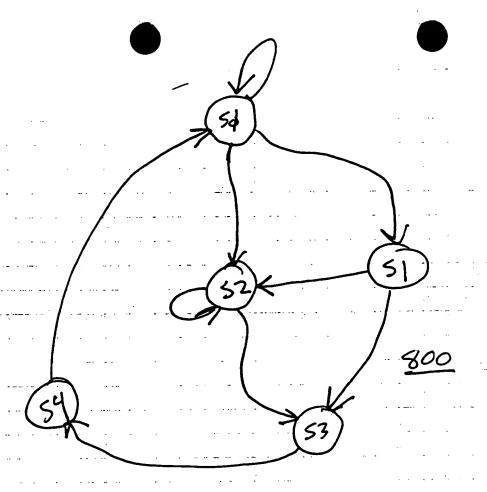


FIG. 8 (Prior And 8A (Prior Art)

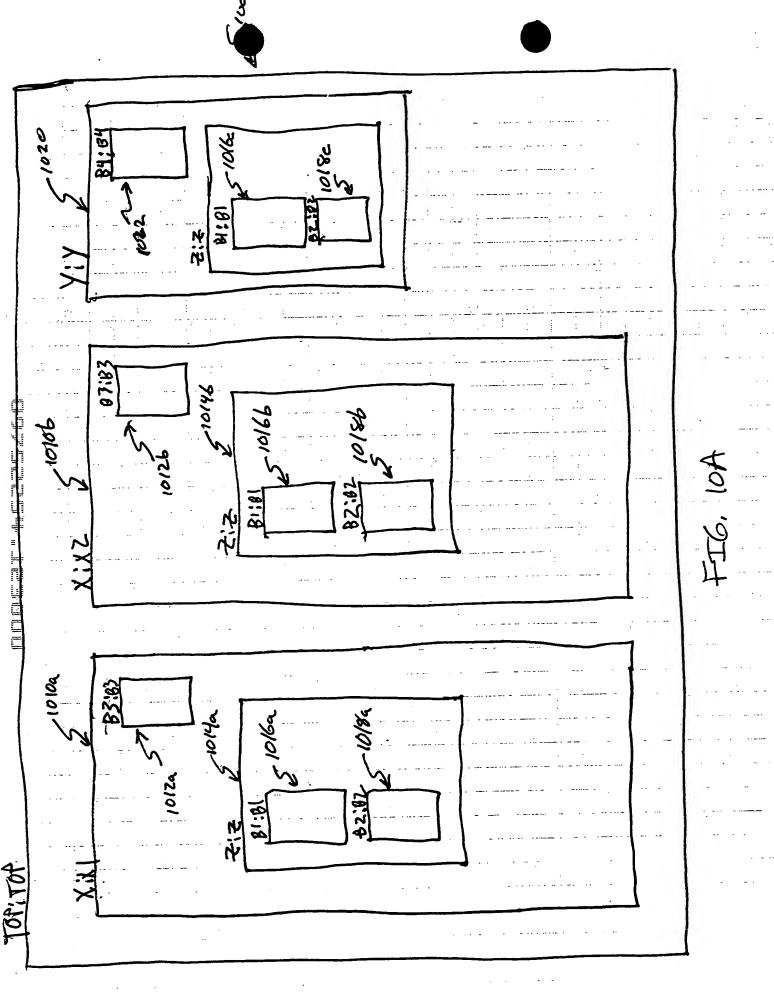
· (Prior Art)

entity Frm Is PORT (... ports for outily Ism. ARCHETECTURE FSM of FSM IS BEGIN ... HDL cacle For FSM and restofthe entity ... fsm-state(0 to 2) = ... signal 801 --!! Embedded FSM: example FSM; --!! clack : (FSM_clock); state_vector states : (50,51,52,53,54); 8 state-encosing: (600, 001, 000, 011, 100 arcs: (50=>56,50=>51,50=>52 65842 -- !! end Fsm;

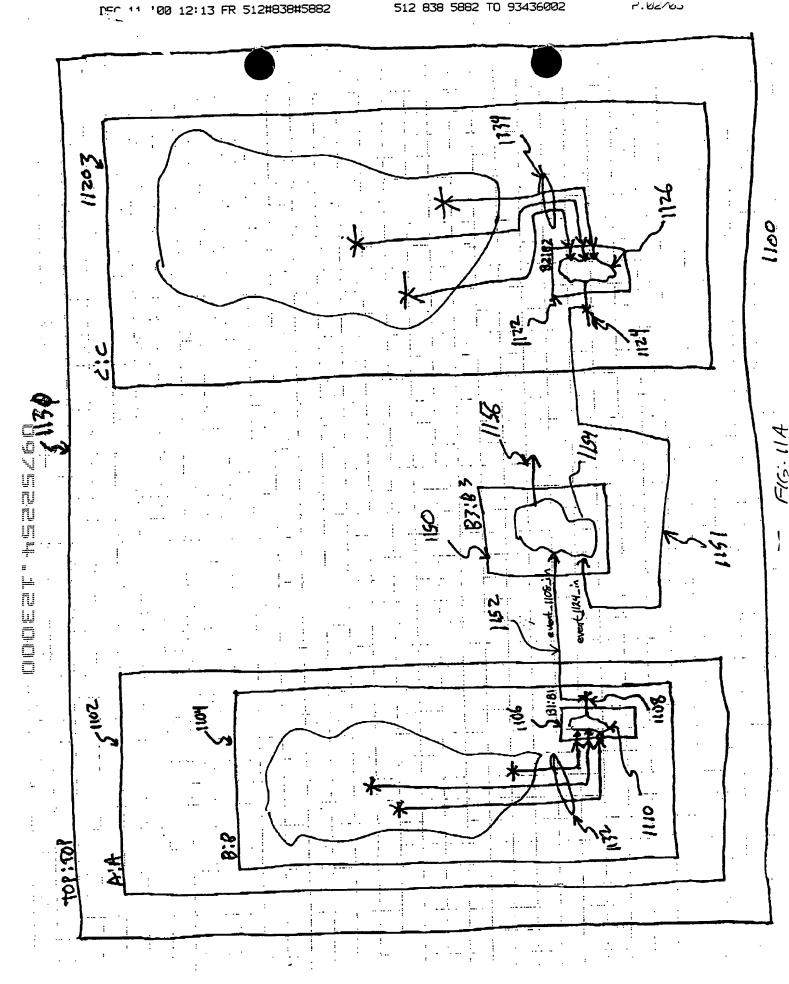
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THY FSM: FSM Formatatelo. Hexample Form House

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